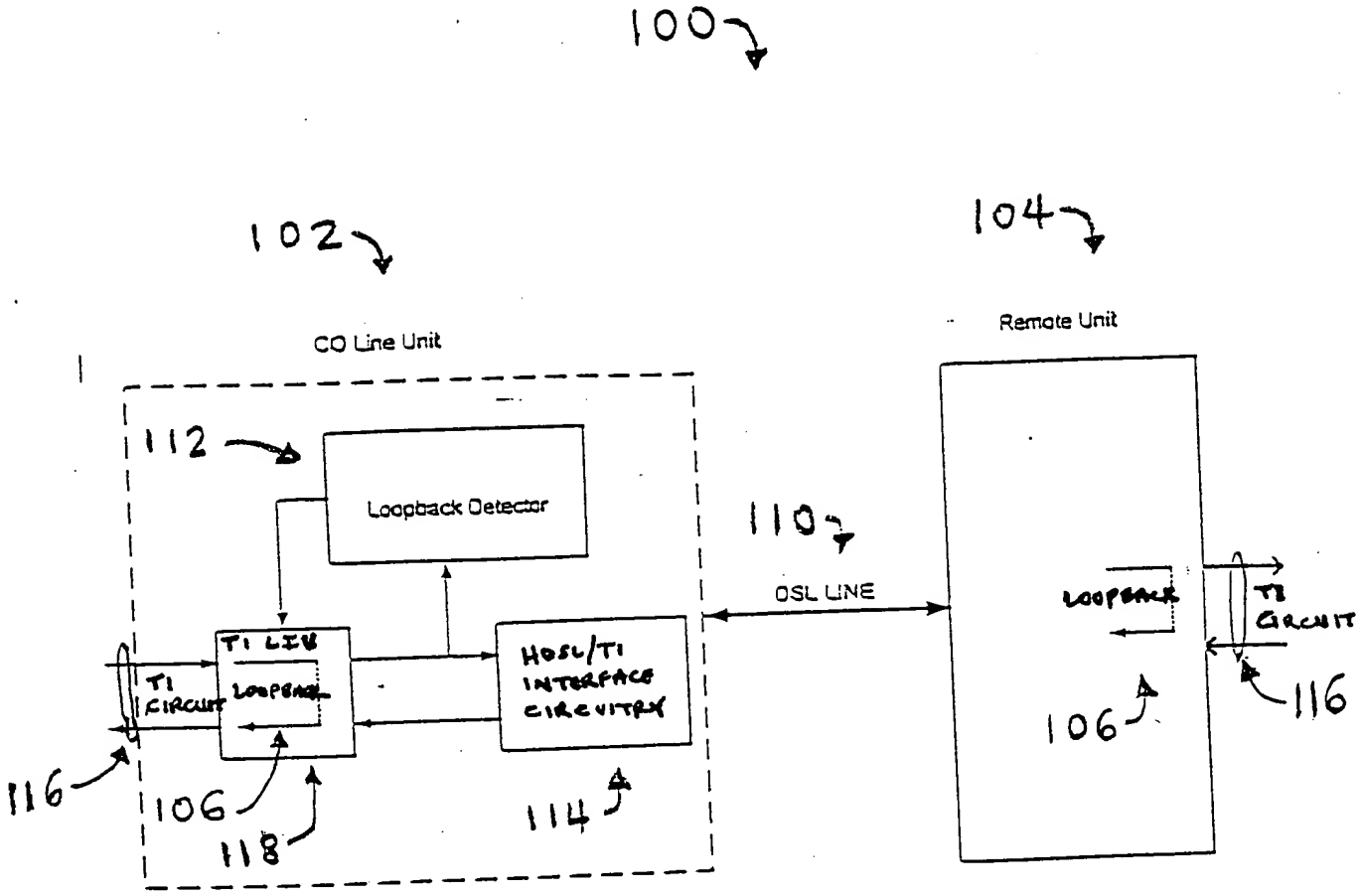

FIG. 1 (PRIOR ART)

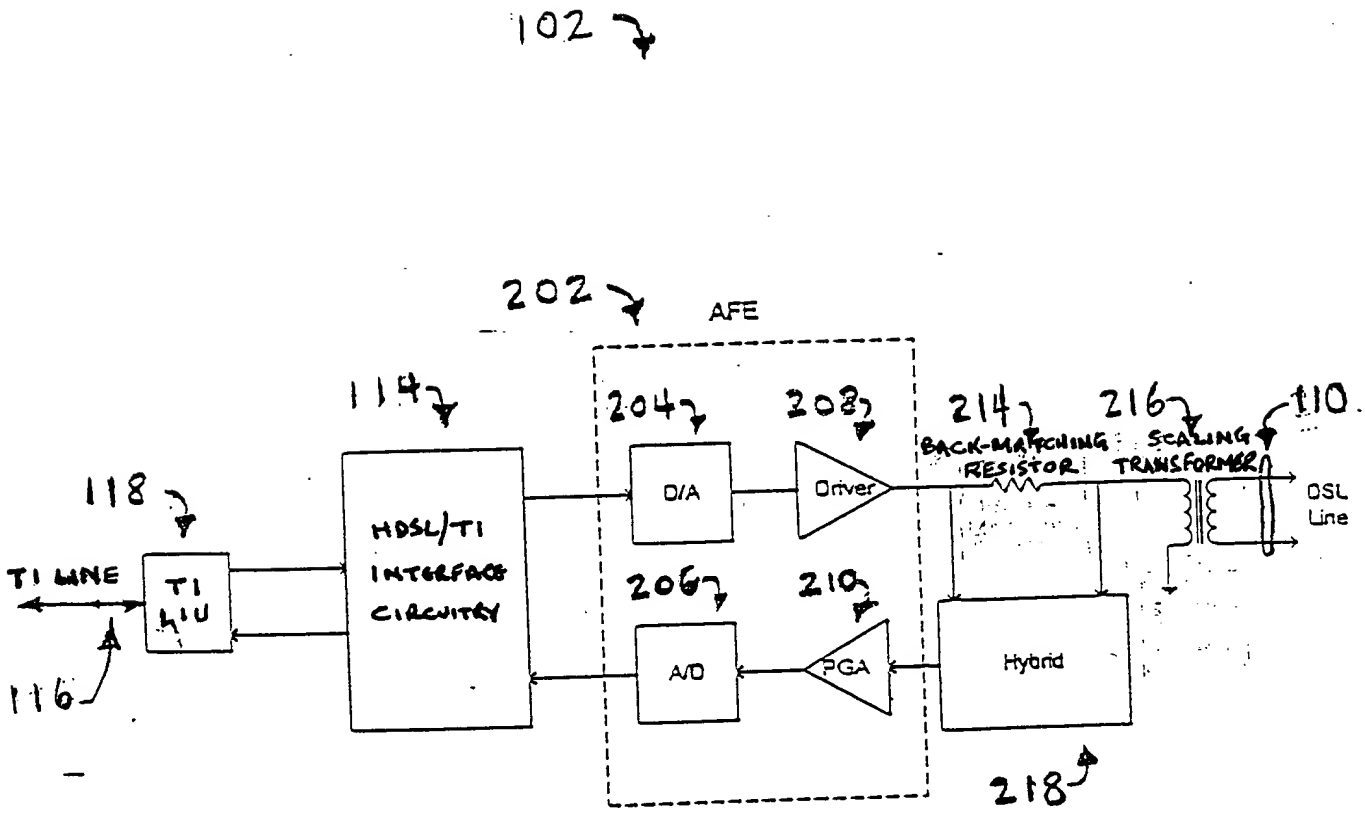

FIG. 2 (PRIOR ART)

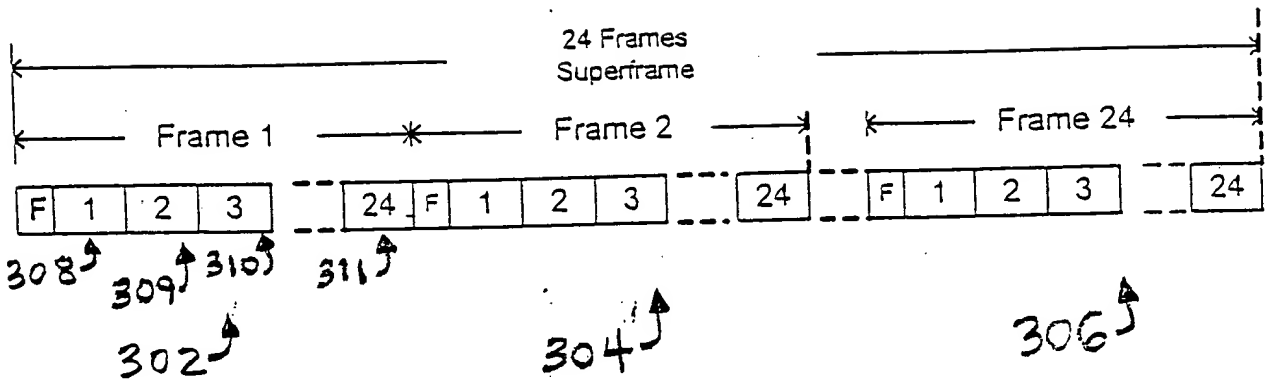

FIG. 3 (PRIOR ART)

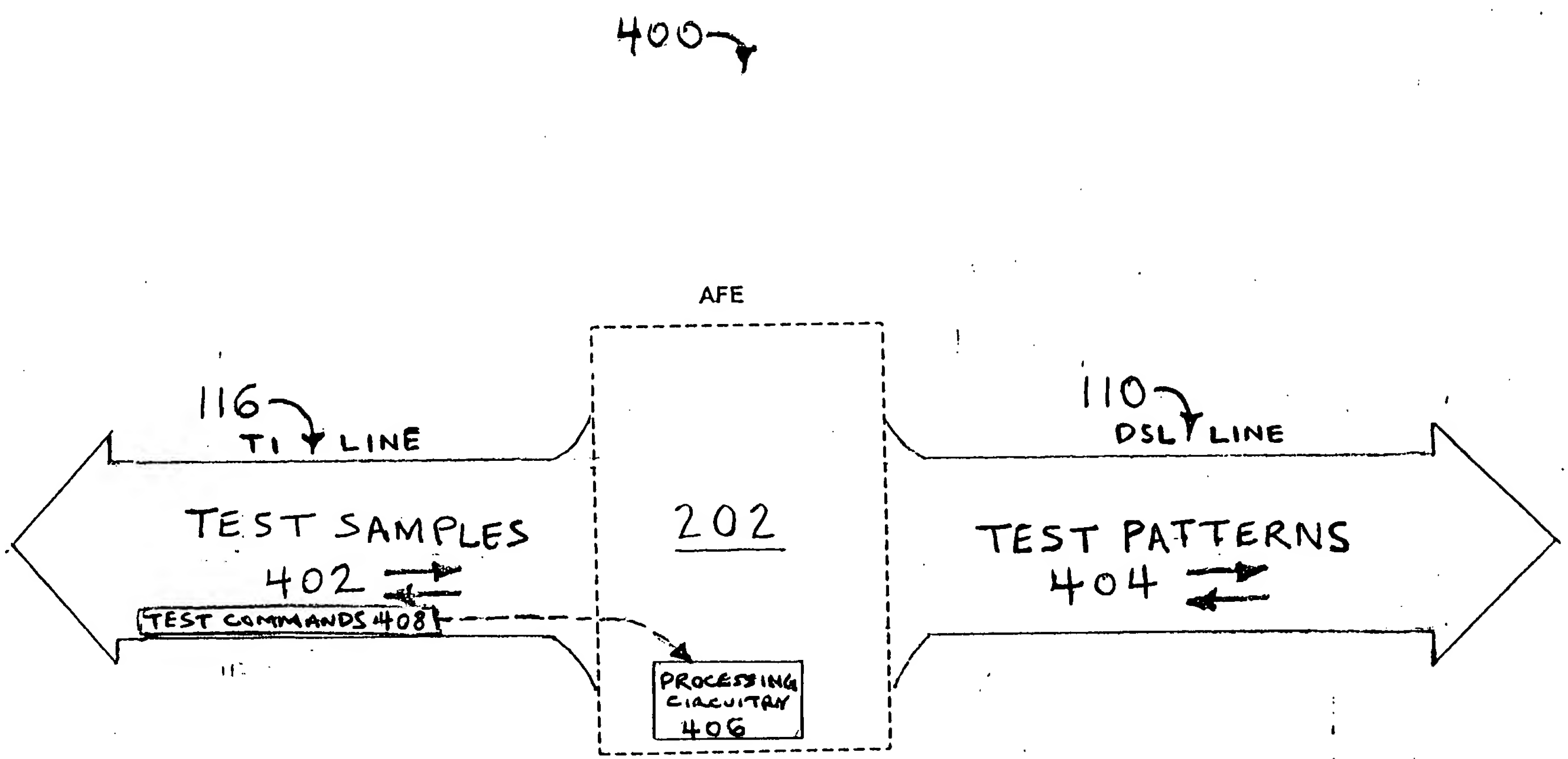
400
AFE
116
T1 LINE
TEST SAMPLES
402
TEST COMMANDS 408
202
PROCESSING CIRCUITRY 406
110
DSL LINE
TEST PATTERNS
404

FIG. 4

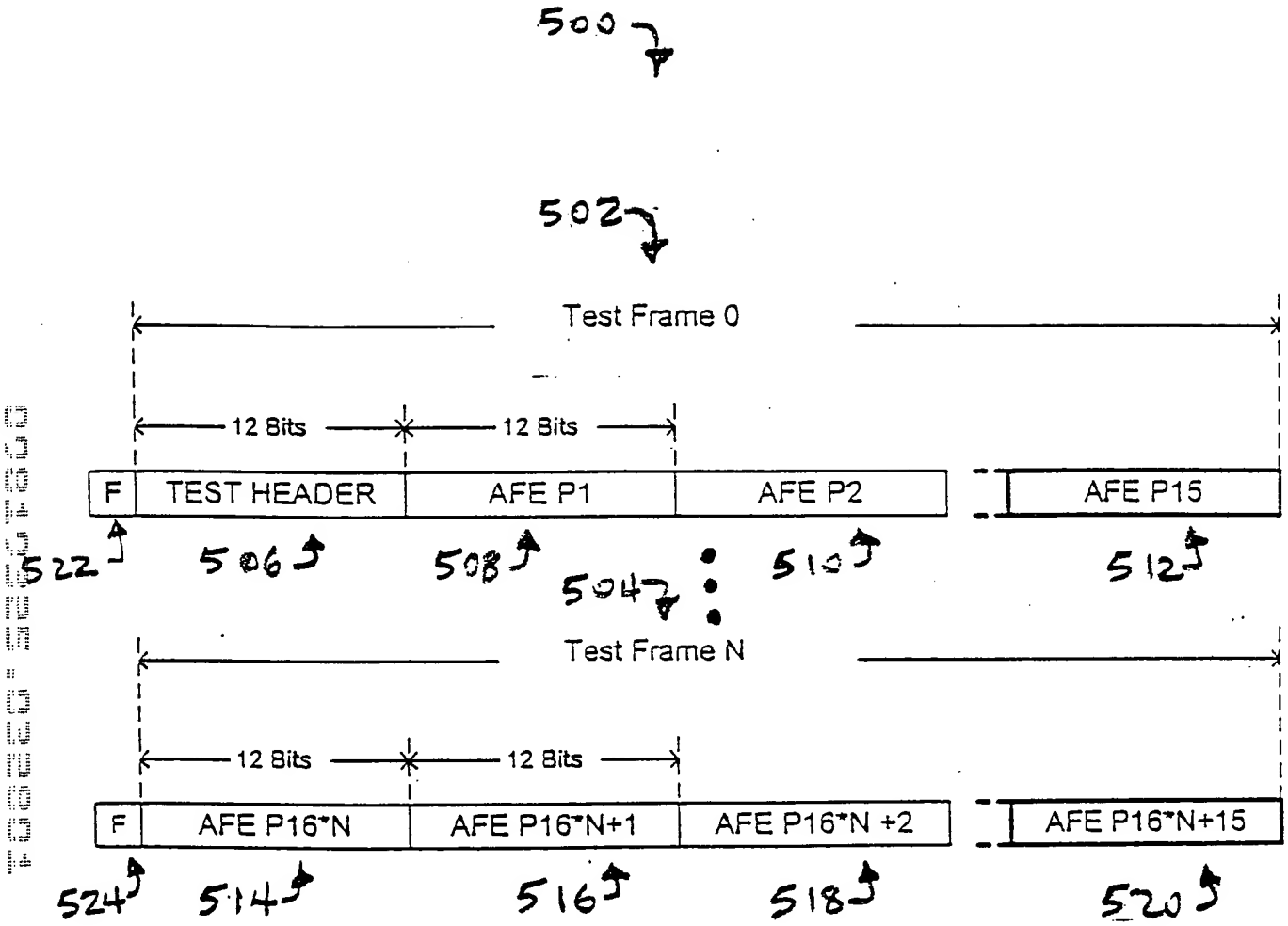
500
502
Test Frame 0
12 Bits
12 Bits
F
TEST HEADER
AFE P1
AFE P2
AFE P15
522
506
508
504
510
512
Test Frame N
12 Bits
12 Bits
F
AFE P16*N
AFE P16*N+1
AFE P16*N +2
AFE P16*N+15
524
514
516
518
520

FIG. 5

600

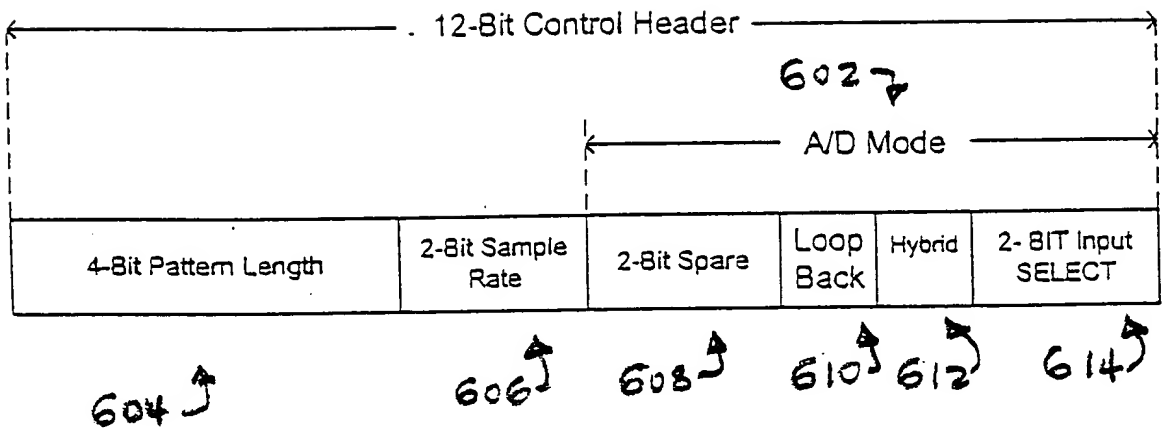
12-Bit Control Header
602
A/D Mode
4-Bit Pattern Length
2-Bit Sample Rate
2-Bit Spare
Loop Back
Hybrid
2- BIT Input SELECT
604
606
608
610
612
614

FIG. 6

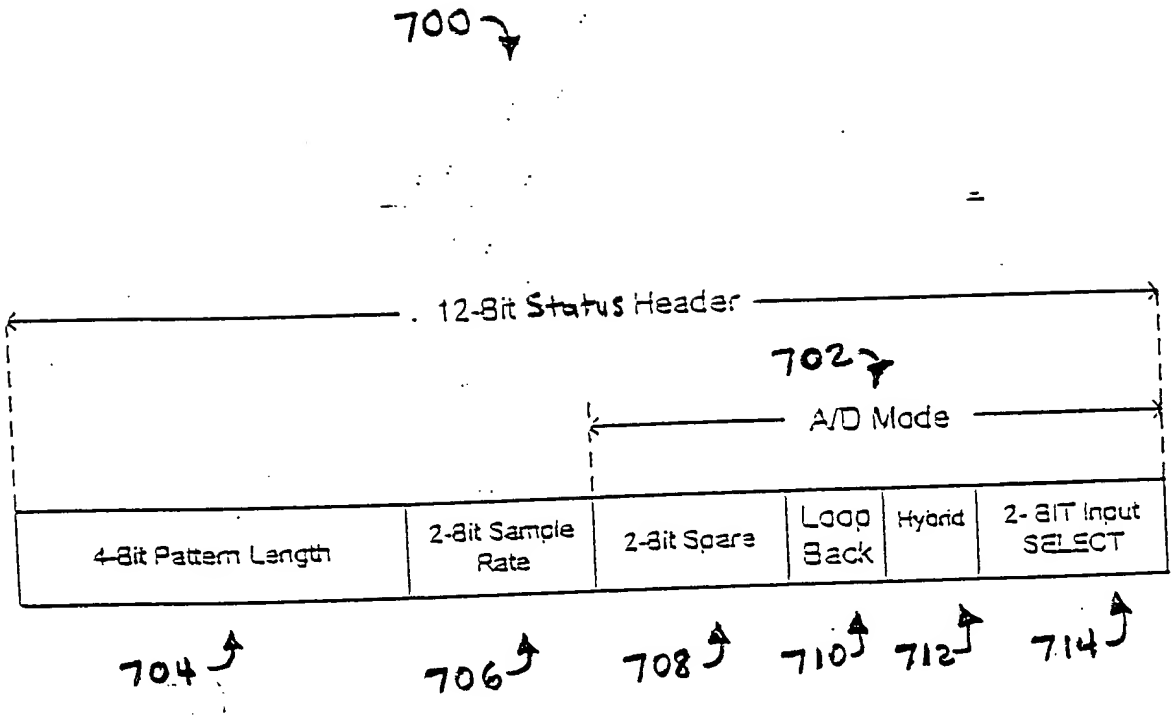
700
12-Bit Status Header
702
A/D Mode
4-Bit Pattern Length
2-Bit Sample Rate
2-Bit Spare
Loop Back
Hybrid
2-BIT Input SELECT
704
706
708
710
712
714

FIG. 7

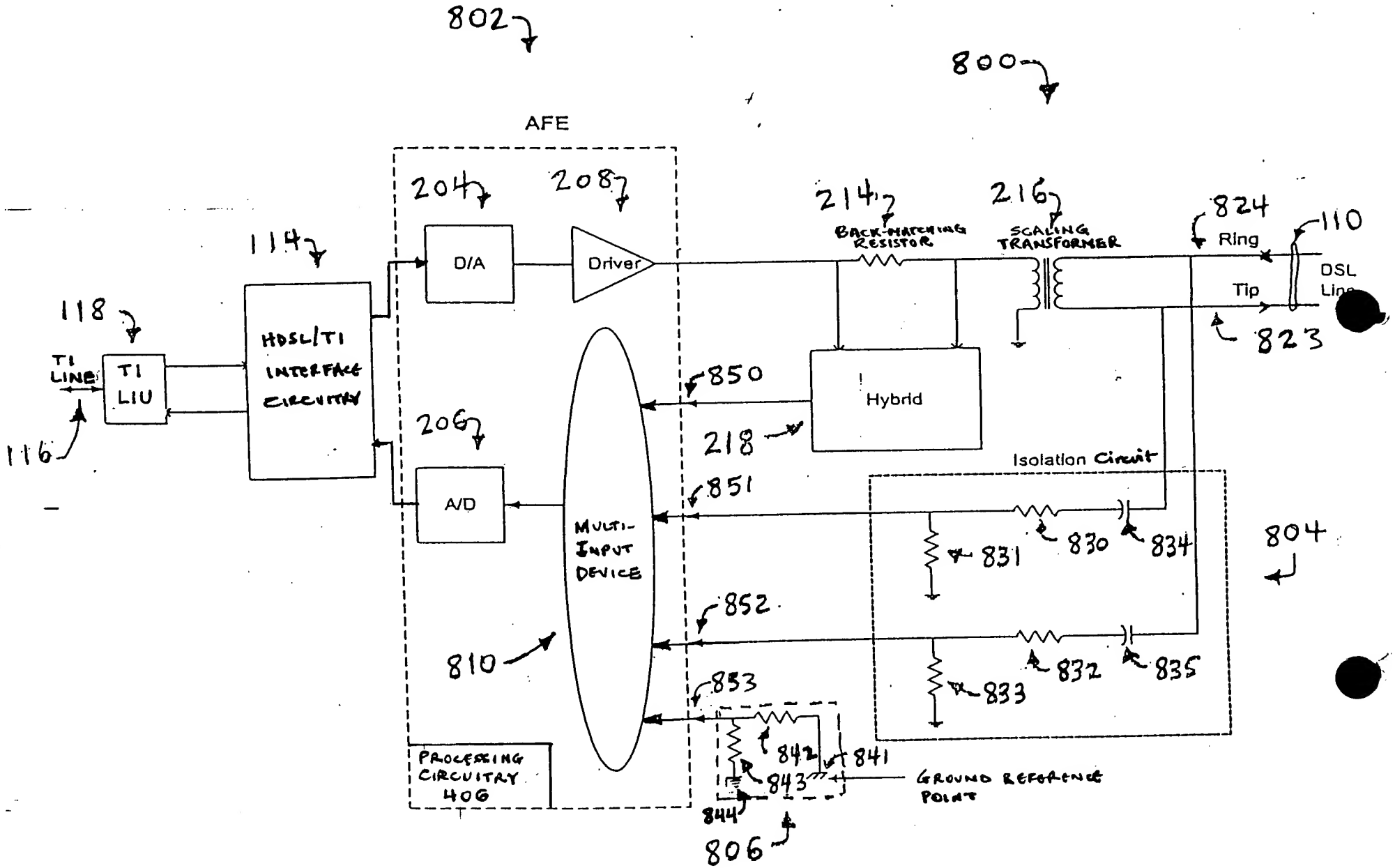
802
800
AFE
204
208
214
BACK-MATCHING RESISTOR
216
SCALING TRANSFORMER
824
Ring
110
DSL Line
Tip
823
114
D/A
Driver
118
TI LINE
TI LIU
HDSL/TI INTERFACE CIRCUITRY
116
850
Hybrid
218
206
A/D
MULTI-INPUT DEVICE
Isolation Circuit
851
831
830
834
804
852
832
835
833
810
853
842
841
843
844
806
PROCESSING CIRCUITRY 406
GROUND REFERENCE POINT

FIG. 8

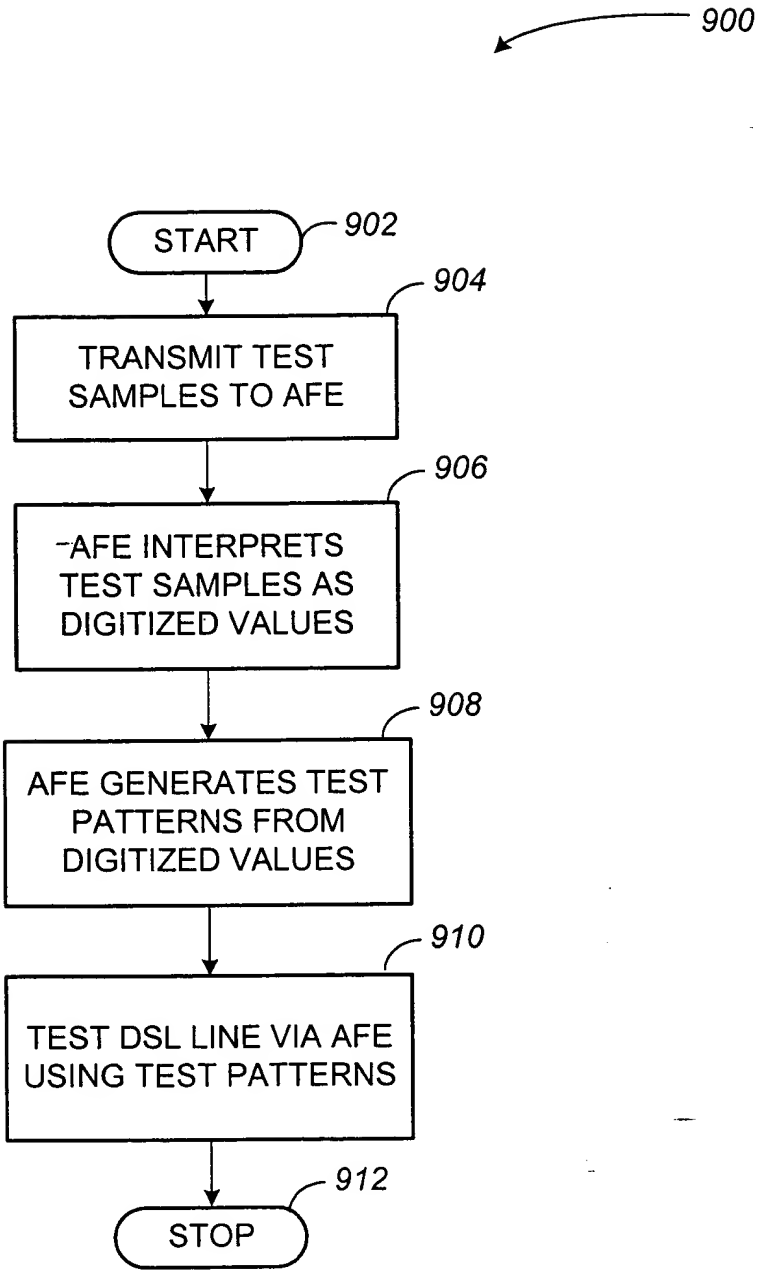
900
START
902
TRANSMIT TEST SAMPLES TO AFE
904
AFE INTERPRETS TEST SAMPLES AS DIGITIZED VALUES
906
AFE GENERATES TEST PATTERNS FROM DIGITIZED VALUES
908
TEST DSL LINE VIA AFE USING TEST PATTERNS
910
STOP
912

FIG. 9

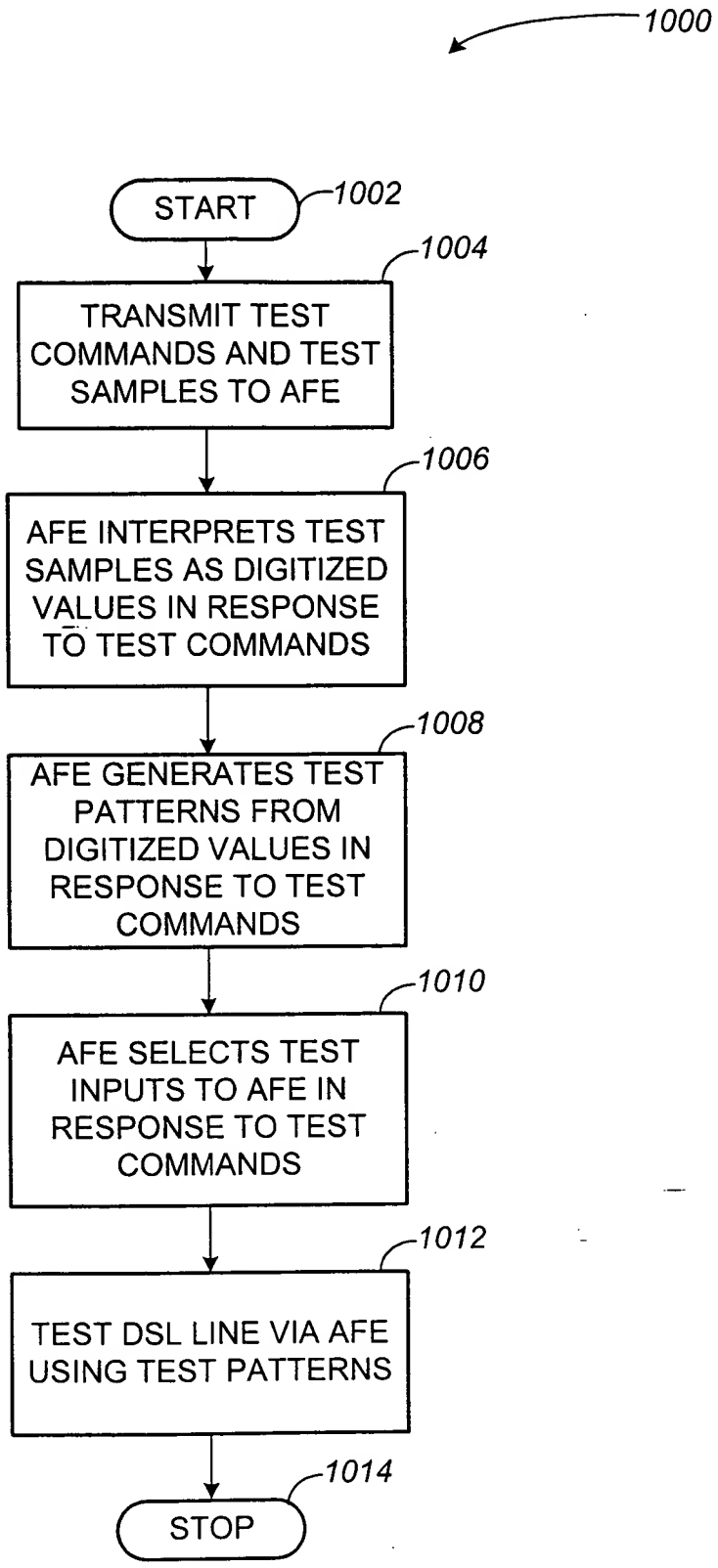
1000
START
1002
TRANSMIT TEST COMMANDS AND TEST SAMPLES TO AFE
1004
AFE INTERPRETS TEST SAMPLES AS DIGITIZED VALUES IN RESPONSE TO TEST COMMANDS
1006
AFE GENERATES TEST PATTERNS FROM DIGITIZED VALUES IN RESPONSE TO TEST COMMANDS
1008
AFE SELECTS TEST INPUTS TO AFE IN RESPONSE TO TEST COMMANDS
1010
TEST DSL LINE VIA AFE USING TEST PATTERNS
1012
STOP
1014

FIG. 10